//SRock

iBOX-280

User Manual

Version 1.0 Published February 2014 Copyright©2014 ASRock Inc. All rights reserved.

Copyright Notice:

No part of this documentation may be reproduced, transcribed, transmitted, or translated in any language, in any form or by any means, except duplication of documentation by the purchaser for backup purpose, without written consent of ASRock Inc.

Products and corporate names appearing in this documentation may or may not be registered trademarks or copyrights of their respective companies, and are used only for identification or explanation and to the owners' benefit, without intent to infringe.

Disclaimer:

Specifications and information contained in this documentation are furnished for informational use only and subject to change without notice, and should not be constructed as a commitment by ASRock. ASRock assumes no responsibility for any errors or omissions that may appear in this documentation.

With respect to the contents of this documentation, ASRock does not provide warranty of any kind, either expressed or implied, including but not limited to the implied warranties or conditions of merchantability or fitness for a particular purpose.

In no event shall ASRock, its directors, officers, employees, or agents be liable for any indirect, special, incidental, or consequential damages (including damages for loss of profits, loss of business, loss of data, interruption of business and the like), even if ASRock has been advised of the possibility of such damages arising from any defect or error in the documentation or product.



This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) this device may not cause harmful interference, and
- (2) this device must accept any interference received, including interference that may cause undesired operation.

CALIFORNIA, USA ONLY

The Lithium battery adopted on this motherboard contains Perchlorate, a toxic substance controlled in Perchlorate Best Management Practices (BMP) regulations passed by the California Legislature. When you discard the Lithium battery in California, USA, please follow the related regulations in advance.

"Perchlorate Material-special handling may apply, see <u>www.dtsc.ca.gov/hazardouswaste/</u> <u>perchlorate</u>"

ASRock's Website: www.ASRock.com

Replaceable batteries

CAUTION

RISK OF EXPLOSION IF BATTERY IS REPLACED BY AN INCORRECT TYPE. DISPOSE OF USED BATTERIES ACCORDING TO THE INSTRUCTIONS

Contact Information

If you need to contact ASRock or want to know more about ASRock, you're welcome to visit ASRock's website at www.ASRock.com; or you may contact your dealer for further information.

ASRock Incorporation

6F., No.37, Sec. 2, Jhongyang S. Rd., Beitou District,

Taipei City 112, Taiwan (R.O.C.)

Contents

Cha	pter 1 Introduction	1
1.1	Package Contents	1
1.2	Product Specifications	2
Cha	pter 2 Product Overview	3
2.1	Inside View	3
2.2	Front View	4
2.3	Rear View	5
Cha	pter 3 Hardware Installation	6
3.1	Removing the Chassis Top Cover	7
3.2	Installing Memory Modules (SO-DIMM)	8
3.3	Installing the Hard Drive	9
Cha	pter 4 Motherboard	14
4.1	Motherboard Layout	14
4.2	Motherboard Specifications	16
4.3	Jumpers Setup	18
4.4	Onboard Headers and Connectors	21
4.5	Expansion Slots (PCI Express, mini-PCIe and mini-PCIe/	27
	mini-SATA Slots)	27

Chapter 1 Introduction

Thank you for purchasing iBOX-280, a reliable embedded box PC produced under ASRock's consistently stringent quality control. It delivers excellent performance with robust design conforming to ASRock's commitment to quality and endurance.

Because the hardware specifications might be updated, the content of this documentation will be subject to change without notice. In case any modifications of this documentation occur, the updated version will be available on ASRock's website without further notice. If you require technical support related to this product, please visit our website for specific information about the model you are using. ASRock's Website: www.asrock.com



The illustrations shown in this manual are examples only, the actual system may differ slightly.

1.1 Package Contents

- iBOX-280
- DN2800MT (pre-installed motherboard)
- 1 x SATA 1 to 1 Power Cable
- Rubber Pads
- 4 x HDD Screws (M3x3)
- mSATA/miniPCIE Screws (M2x3)
- Wall Mount Bracket (optional)
- Power Adapter
- User Manual



If any items are missing or appear damaged, contact your authorized dealer.

1.2 Product Specifications

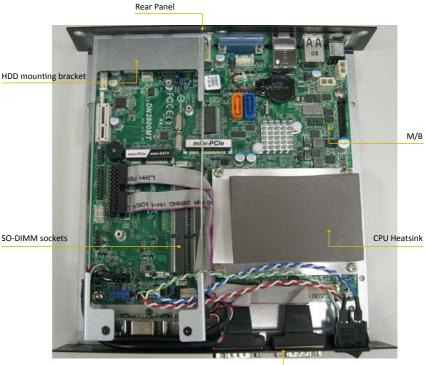
iBOX-280			
Processor System			
CPU	Intel Cedarview Atom N2800 Dual core 1.86GHz TDP 6.5W		
Memory	2 x DDR3-1066MHz SO-DIMM up to 4 GB		
Chipset	Intel NM10		
Graphic	Intel GMA3650		
LAN Chipset	Intel 82574L		
Watch Dog	256 Segments,0,1,2,255sec/min		
Rear I/O			
Serial Port	2 x 232 port		
USB	6 USB 2.0 ports		
LAN	1 RJ45 Port for Gbe		
Vedio output	1 x VGA, 1 x HDMI		
Audio	Mic-in/ Line out		
Expansion	1 x mini PCIe /1 x mSATA		
Storage			
Type 1 x 2.5" HDD/ SSD			
OS Support			
Window 7 / Linux	C C C C C C C C C C C C C C C C C C C		
Certifications			
CE, FCC, Class A			
Environmental			
Operating Temp	0°C~50°C		
Storage Temp	-20°C~80°C		
Humidity	10%~90%		
Mechanical			
Material	Top cover -aluminum extrusion/ Base- metal		
Dimension	200 x 200 x 35mm		
Weight	1.8 Kg		
Mounting	mounting bracket (optional)		

* For detailed product information, please visit our website: <u>http://www.asrock.com</u>

Chapter 2 Product Overview

This chapter provides diagrams showing the location of important components of the iBOX-280.

2.1 Inside View



Front Panel

2.2 Front View



	Description
1	2 x USB 2.0 Ports
2	2 x COM Ports
3	Power LED
4	HDD LED
5	On-/off Switch

Status LED Definitions

Power LED	
Status	Description
Solid Green	Power on
Off	Power off
HDD Status LED	
Status	Description
Red	HDD installed
Off	HDD uninstalled

2.3 Rear View



No.	Description	No.	Description
1	Antenna Port	6	Line out (Lime)
2	LAN RJ-45 Port (LAN1)*	7	HDMI Port (HDMI1)
3	VGA Port (VGA1)	8	4 x USB 2.0 Ports
4	Antenna Port	9	DC Jack (DC_JACK1)
5	Microphone (Pink)		

* There are two LEDs on each LAN port. Please refer to the table below for the LAN port LED indications.

ACT/LINK LED



LAN Port

Activity / Link LED		Speed LED	
Status	Description	Status	Description
Off	No Link	Off	10Mbps connection
Off	Data Activity	Orange	100Mbps connection
On	Link	Green	1Gbps connection

English

Chapter 3 Hardware Installation

This chapter provides step-by-step procedures on how to install components.

Installation Procedures



Removing the chassis top cover

Installing the memory modules (SO-DIMM)

Installing the 2.5-inch hard drive

Replacing the chassis top cover

After making sure that you have properly connected the power supply and all the necessary peripherals, power on the system.

3.1 Removing the Chassis Top Cover

- 1. Remove the three screws on the front panel.
- 2. Remove the three screws on the rear panel.
- 3. Remove the four screws in the bottom case.
- 4. Lift up and remove the top cover.

0 2 6

5.

3.2 Installing Memory Modules (SO-DIMM)

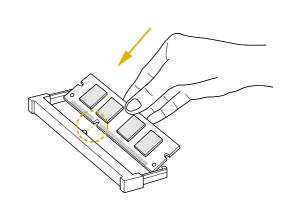
This motherboard provides two 204-pin DDR3 (Double Data Rate 3) SO-DIMM slots. Please install the SO-DIMM module into the DDR3_A2 for the first priority.



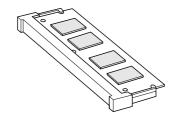
It is not allowed to install a DDR or DDR2 memory module into a DDR3 slot; otherwise, this motherboard and SO-DIMM may be damaged.



The SO-DIMM only fits in one correct orientation. It will cause permanent damage to the motherboard and the SO-DIMM if you force the SO-DIMM into the slot at incorrect orientation.







iBox

3.3 Installing the Hard Drive

Removing HDD Mounting Bracket

- 1. Remove the four screws that secure the HDD mounting bracket to the chassis.
- 2. Lift up and remove the HDD mounting bracket.





Installing a 2.5-inch Hard Drive

- 1. Place the HDD into the HDD mounting bracket with the printed circuit board side facing down. Carefully align the mounting holes in the hard drive and the HDD carrier.
- 2. Secure the hard drive into the place using the four screws.
- 3. Attach one end of the SATA 1 to 1 Power Cable to the hard drive.
- 4. Secure the HDD mounting bracket to the chassis using the four screws.
- 5. Attach the SATA data cable and power cable to the motherboard.



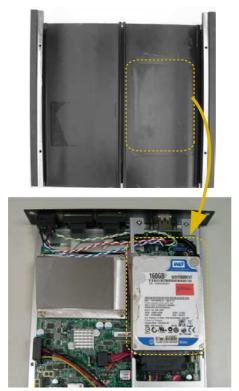
English

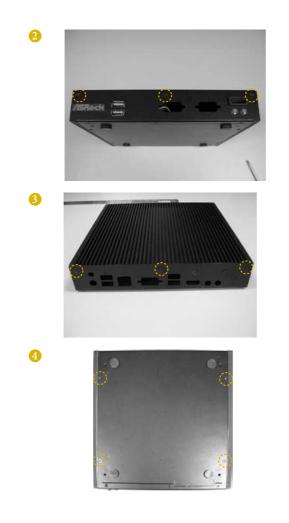
iBox

3.4 Replacing the Top Cover

- 1. Replace the top cover, making sure the mark on the top cover is aligned with the HDD mounting bracket.
- 2. Secure the three screws on the front panel.
- 3. Secure the three screws on the rear panel.
- 4. Secure the four screws at the bottom.

0





3.5 Using the Wall Mount Bracket

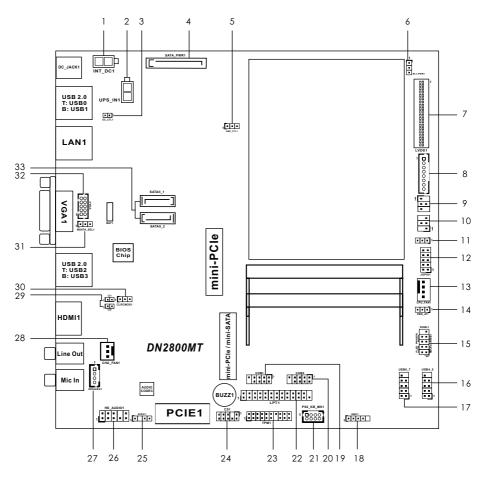
- 1. Attach the Wall Mount Bracket to the base of iBOX-280 using the four screws (M3x4)
- 2. Mount the iBOX-280 to the wall using the four screws (M3x4).





Chapter 4 Motherboard

4.1 Motherboard Layout



No.	Description
1	2-pin ATX Power Input/Output Connector
2	2-pin UPS Module Power Input Connector
3	DC_CTL1
4	SATA Power Output Connector
5	AMP_CTL1
6	BLT_PWM1
7	LVDS Panel Connector
8	BLT_CTL1
9	PNL_PWR1
10	BKT_PWR1
11	Digital Input / Output Power Select
12	Digital Input / Output Pin Header
13	4-Pin CPU FAN Connector
14	ATX/AT mode Selection
15	System Panel Header
16	USB2.0 Header (USB4_5)
17	USB2.0 Header (USB6_7)
18	DMIC1
19	RS-232 Port 4 Pin Header (COM1)
20	RS-232 Port 4 Pin Header (COM2)
21	PS2_KB_MS1
22	Printer Port Header
23	TPM Header
24	CS1
25	SPDIF1
26	Front Panel Audio Header
27	3W Audio AMP Output Wafer
28	3-Pin Chassis FAN Connector
29	Chassis Intrusion Headers (CI1, CI2)
30	Clear CMOS Header
31	MSATA_SEL1
32	VGA2
33	SATA2 Connectors (SATAII_1, SATAII_2)

4.2 Motherboard Specifications

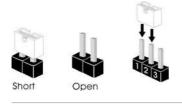
Form Factor	Dimensions	Mini-ITX (6.7-in x 6.7-in)		
	Dimensions	- Intel Dual-Core Atom TM CedarView Processor N2800		
	CPU			
		- Supports Hyper-Threading Technology		
Processor	Core Number	2		
System	Max Speed	N2800: 1.86 GHz		
•	L3 Cache	N/A		
	Chipset	NM10		
BIOS UEFI				
	PCI	0		
	Mini-PCIe	1 (Half Size) + 1 (Full Size, shared with m-SATA)		
Expansion	mSATA	1 (share with mini-PCIe)		
Slot	PCIe	1 (x1)		
	CFast Card	0		
	Socket	о 		
	Technology	Single Channel DDR3 800/1066 MHz SDRAM		
Memory	Max.	4GB		
	Socket	2 x SODIMM		
	Controller	Intel [®] PowerVR SGX545, Support Directx9 compliant		
	Controner	Pixel Shader v3.0 and OGL 3.0		
	VRAM	Shared Memory		
	VGA	Supports max. resolution 1920 x 1200		
Graphics	LVDS	Dual channel 24-bit, max resolution 1920 x 1200@60Hz		
	HDMI	1		
	DVI	No		
	DisplayPort	No		
	Multi Display	Yes (Dual Display)		
	Ethernet	10/100/1000 Mbps		
Ethernet	Controller	GbE LAN: 1 x Intel [®] 82574L		
	Connector	1 x RJ-45		
	Max Data	SATA2 (3.0Gb/s)		
SATA	Transfer Rate			
	VGA	1		
	DVI	0		
	HDMI	1		
	DisplayPort	0		
Rear I/O	Ethernet	1		
	USB	4		
	Audio	2 (Mic-In, Line-Out)		
	Serial	0		
	PS/2	0		
		*		

	USB	4 (USB 2.0 compliant)
	LVDS/Inverter	
	VGA	1 (shared with rear I/O VGA COM)
	Serial	2 (RS232) / 4 from TPM header
	SATA	2 x SATA2 (3.0Gb/s)
	mPCIe	1 + 1 shared
Internal	Parallel	1
Connector	mSATA	1 shared
	IrDA	0
	GPIO 8-bit	4 in / 4 out
	SATA PWR	1
	Output Con	1
	Speaker	1
	Header	1
Watchdog	Output	From Super I/O to drag RESETCON#
Timer	Interval	256 Segments, 0,1,2255 Sec/Min
	Input PWR	9~19V DC-In (DC-Jack or 2-pin PWR Con)
Power		AT/ATX Supported
Requirements	Power On	-AT : Directly PWR on as power input ready
		-ATX : Press button to PWR on after power input ready
Environment	Temperature	0°C – 60°C

* For detailed product information, please visit our website: <u>http://www.asrock.com</u>

4.3 Jumpers Setup

The illustration shows how jumpers are setup. When the jumper cap is placed on the pins, the jumper is "Short". If no jumper cap is placed on the pins, the jumper is "Open". The illustration shows a 3-pin jumper whose pin1 and pin2 are "Short" when a jumper cap is placed on these 2 pins.

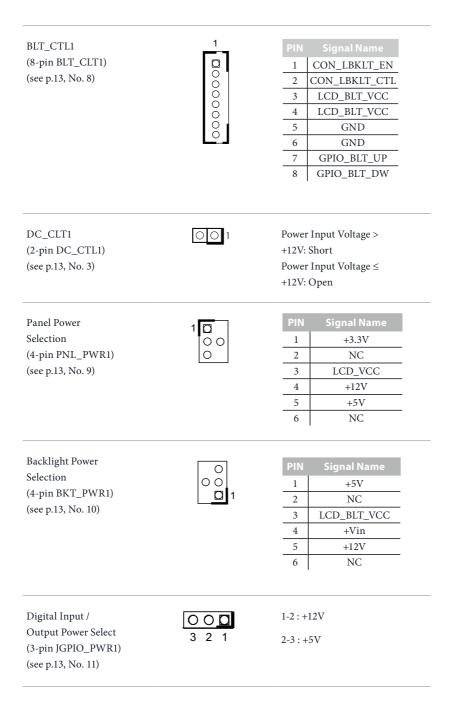


Clear CMOS Jumper (CLRCMOS1) (see p.13, No. 30)



CLRCMOS1 allows you to clear the data in CMOS. To clear and reset the system parameters to default setup, please turn off the computer and unplug the power cord from the power supply. After waiting for 15 seconds, use a jumper cap to short pin2 and pin3 on CLRCMOS1 for 5 seconds. However, please do not clear the CMOS right after you update the BIOS. If you need to clear the CMOS when you just finish updating the BIOS, you must boot up the system first, and then shut it down before you do the clear-CMOS action. Please be noted that the password, date, time, and user default profile will be cleared only if the CMOS battery is removed.

AMP_CTL1 (3-pin AMP_CTL1) (see p.13, No. 5)	$\begin{array}{c} \Box \bigcirc \bigcirc \\ 1 & 2 & 3 \end{array}$	PINSignal Name1GPIO_VOL_DW2GND3GPIO_VOL_UP
BLT_PWM1 (CON_LBKLT_CTL) (3-pin BLT_PWM1) (see p.13, No. 6)		1-2 : +3V 2-3 : +5V



ATX/AT Mode Selection (3-pin PWR_JP1) (see p.13, No. 14)	00 0 321	1-2 : AT Mode 2-3 : ATX Mode
MSATA_SEL1 (Disable SATAII_2) (3-pin MSATA_ SEL1) (see p.13, No. 31)		1-2 : mPCIE 2-3 : mSATA

4.4 Onboard Headers and Connectors

2 1 1

40

39

 \wedge

Onboard headers and connectors are NOT jumpers. Do NOT place jumper caps over these headers and connectors. Placing jumper caps over the headers and connectors will cause permanent damage to the motherboard.

LVDS Panel
Connector
(40-pin LVDS1)
(see p.13, No. 7)

$\begin{array}{c ccccccccccccccccccccccccccccccccccc$				
$\begin{array}{c cccc} 4 & \text{LDDC_CLK} & 3 & +3V \\ \hline & 1VDS_A_ \\ DATA0# & 5 & \text{LDDC_DATA} \\ \hline & DATA0# & 7 & DATA0 \\ \hline & DATA0 & 7 & DATA0 \\ \hline & 10 & 1VDS_A_ \\ 0 & DATA1 & 9 & DATA1# \\ \hline & 12 & 1VDS_A_ \\ DATA2# & 11 & GND \\ \hline & 14 & GND & 13 & 1VDS_A_ \\ 14 & GND & 13 & DATA2 \\ \hline & 14 & GND & 13 & 1VDS_A_ \\ 14 & GND & 13 & 1VDS_A_ \\ 16 & 1VDS_A_ \\ 17 & 0ATA3 & 12 & 0ATA3# \\ \hline & 18 & 1VDS_A_CLK# & 17 & GND \\ \hline & 20 & GND & 19 & 1VDS_A_CLH \\ \hline & 1VDS_B_ \\ 22 & DATA0 & 21 & 0ATA0# \\ \hline & 1VDS_B_ \\ 24 & 1VDS_B_ \\ 24 & 1VDS_B_ \\ 26 & GND & 25 & 0ATA1 \\ \hline & 1VDS_B_ \\ 26 & GND & 25 & 0ATA1 \\ \hline & 1VDS_B_ \\ 28 & 1VDS_B_ \\ 29 & 0ATA2 & 27 & 0ATA2# \\ \hline & 1VDS_B_ \\ 30 & 1VDS_B_ \\ 31 & 1VDS_B_ \\ 32 & GND & 31 & 1VDS_B_ \\ \hline & 1VDS_B_ \\ 34 & 1VDS_B_CLK & 33 & 1VDS_B_CLK \\ \hline & 36 & CON_LBKLT_ \\ 36 & CON_LBKLT_ \\ 58 & 1CD_BLT_VCC & 37 & CON_LBKLT_ \\ CTL & \hline \end{array}$	PIN	Signal Name	PIN	Signal Name
1INDEGRATION0INT6IVDS_A_ DATA0#5IDDC_DATA8GND7IVDS_A_ DATA010IVDS_A_ DATA19IVDS_A_ DATA1#12IVDS_A_ DATA2#11GND14GND13IVDS_A_ DATA316IVDS_A_CLK#17GND20GND19IVDS_A_CLK#22IVDS_B_ DATA1#21DATA0#24IVDS_B_ DATA1#23GND26GND25IVDS_B_ DATA128IVDS_B_ DATA227DATA2#30IVDS_B_ DATA3#29DPIVDD_EN DATA334IVDS_B_CLK33IVDS_B_CLK36CON_LBKLT_ EN35GND38ICD_BLT_VCC37CON_LBKLT_ CTL		LCD_VCC		LCD_VCC
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	4	LDDC_CLK	3	+3V
$\begin{array}{ c c c c c c } \hline DATA0# & & & & & & & & \\ \hline DATA0 & & & & & & & & \\ \hline & & & & & & & & \\ \hline & & & &$	6	LVDS_A_	5	IDDC DATA
8GND7DATA010LVDS_A_ DATA19LVDS_A_ DATA1#12LVDS_A_ DATA2#11GND14GND13LVDS_A_ DATA214GND13LVDS_A_ DATA316LVDS_A_CLK#17GND20GND19LVDS_A_CLF22LVDS_B_ DATA1#21LVDS_B_ DATA024LVDS_B_ DATA1#23GND26GND25LVDS_B_ DATA128LVDS_B_ DATA227DATA2#30LVDS_B_ DATA3#29DPLVDD_EN DATA334LVDS_B_CLK33LVDS_B_CLK36CON_LBKLT_ EN35GND38LCD_BLT_VCC37CON_LBKLT_ CTL	0	DATA0#	5	LDDC_DAIN
$\begin{array}{ c c c c c c } & I & DATA0 \\ \hline DATA1 & P & IVDS_A_ \\ \hline DATA1 & P & DATA1 \\ \hline DATA1 & P & DATA1 \\ \hline DATA2 & 11 & GND \\ \hline DATA2 & 11 & GND \\ \hline DATA2 & 11 & GND \\ \hline DATA2 & 15 & DATA2 \\ \hline DATA2 & 15 & DATA3 \\ \hline DATA2 & 10 & DATA2 \\ \hline 20 & GND & 19 & IVDS_A_CLH \\ \hline 22 & IVDS_B_ & 21 & DATA0 \\ \hline DATA0 & 19 & IVDS_B_ \\ \hline 24 & IVDS_B_ & 23 & GND \\ \hline 26 & GND & 25 & IVDS_B_ \\ \hline DATA1 & 10 & DATA1 \\ \hline 28 & IVDS_B_ & 27 & DATA2 \\ \hline DATA2 & 27 & DATA2 \\ \hline 30 & IVDS_B_ & 29 & DPIVDD_EN \\ \hline 32 & GND & 31 & IVDS_B_ \\ \hline DATA3 & 29 & DATA3 \\ \hline 34 & IVDS_B_CLK & 33 & IVDS_B_CLK \\ \hline 36 & CON_LBKLT_ \\ \hline 38 & ICD_BLT_VCC & 37 & CON_LBKLT \\ \hline 37 & CON_LBKLT \\ \hline 38 & ICD_BLT_VCC & 37 & CON_LBKLT \\ \hline 37 & CTI & CTI \\ \hline \end{array}$	0	CND	7	LVDS_A_
$ \begin{array}{c c c c c c c } \hline 10 & DATA1 & 9 & DATA1# \\ \hline DATA1 & IVDS_A_ & 11 & GND \\ \hline DATA2# & 11 & GND \\ \hline DATA2# & 11 & GND \\ \hline DATA2# & 13 & DATA2 \\ \hline DATA2 & 13 & DATA2 \\ \hline DATA3 & 15 & DATA3# \\ \hline DATA3 & 15 & DATA3# \\ \hline DATA3 & 17 & GND \\ \hline 20 & GND & 19 & IVDS_A_CLH \\ \hline 22 & IVDS_B_ & 21 & IVDS_B_ \\ \hline DATA0 & 21 & DATA0# \\ \hline 24 & IVDS_B_ & 23 & GND \\ \hline 24 & IVDS_B_ & 23 & GND \\ \hline 26 & GND & 25 & IVDS_B_ \\ \hline DATA1# & 23 & DATA1 \\ \hline 28 & IVDS_B_ & 27 & DATA2# \\ \hline DATA2 & 27 & DATA2# \\ \hline 30 & IVDS_B_ & 29 & DPIVDD_EN \\ \hline 32 & GND & 31 & IVDS_B_ \\ \hline 34 & IVDS_B_CLK & 33 & IVDS_B_CLK \\ \hline 36 & CON_LBKLT_ \\ \hline 38 & ICD_BIT_VCC & 37 & CON_LBKLT \\ \hline 38 & ICD_BIT_VCC & 37 & CON_LBKLT \\ \hline \end{array}$	0	GND	/	DATA0
$\begin{array}{ c c c c c } & DATA1 & I & DATA1# \\ \hline DATA2 & I & GND \\ \hline DATA2 & 11 & GND \\ \hline DATA2 & 13 & LVDS_A \\ \hline DATA2 & 13 & DATA2 \\ \hline DATA3 & 15 & DATA3 \\ \hline DATA3 & 10 & DATA3 \\ \hline DATA3 & 10 & DATA2 \\ \hline DATA3 & 10 & DATA3 \\ \hline DATA3 & 10 & DATA3 \\ \hline DATA3 & 10 & DATA3 \\ \hline 20 & GND & 19 & LVDS_A_CLH \\ \hline 20 & GND & 19 & LVDS_B_C \\ \hline 20 & GND & 19 & LVDS_B_C \\ \hline 20 & GND & 19 & LVDS_B_C \\ \hline 22 & DATA0 & 21 & DATA0 \\ \hline 24 & LVDS_B_ & 23 & GND \\ \hline 24 & LVDS_B_ & 23 & DATA1 \\ \hline 26 & GND & 25 & LVDS_B_ \\ \hline DATA1 & 1VDS_B_ & 27 & DATA2 \\ \hline 30 & LVDS_B_ & 27 & DATA2 \\ \hline 30 & LVDS_B_ & 29 & DPLVDD_EN \\ \hline 32 & GND & 31 & LVDS_B_ \\ \hline 34 & LVDS_B_CLK & 33 & LVDS_B_CLK \\ \hline 36 & CON_LBKLT_ & 35 & GND \\ \hline 38 & LCD_BLT_VCC & 37 & CON_LBKLT_ \\ \hline CTL & \hline \end{array}$	10	LVDS_A_	0	LVDS_A_
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	10	DATA1	9	DATA1#
$\begin{array}{ c c c c c } \hline DATA2# & & & & \\ \hline DATA2# & & & & \\ \hline DATA2 & & & \\ \hline & & & & \\ \hline &$	10	LVDS_A_		OND
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	12	DATA2#	11	GND
$ \begin{array}{ c c c c c c } & LVDS_A_{-} & LVDS_A_{-} \\ \hline DATA3 & IVDS_A_{-} \\ \hline DATA3 & IVDS_A_{-} \\ \hline DATA0 & IVDS_A_{-} \\ \hline DATA0 & IVDS_A_{-} \\ \hline DATA0 & IVDS_B_{-} \\ \hline DATA0 & IVDS_B_{-} \\ \hline DATA1 & IVDS_B_{-} \\ \hline DATA1 & IVDS_B_{-} \\ \hline DATA1 & IVDS_B_{-} \\ \hline DATA2 & IVDS_B_{-} \\ \hline DATA2 & IVDS_B_{-} \\ \hline DATA2 & IVDS_B_{-} \\ \hline DATA3 & IVDS_B_{-} \\ \hline DATA3 & IVDS_B_{-} \\ \hline DATA3 & IVDS_B_{-} \\ \hline ATA3 & IVDS_{-} \\ \hline ATA3 & IITA3 & IITA3 \\ \hline ATA3 & IITA3 & IITA3 & IITA3 \\ \hline ATA3 & IITA3 & IITA3 & IITA3 & IITA3 & $		CNID	10	LVDS_A_
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	14	GND	13	DATA2
$\begin{array}{ c c c c c c c } \hline DATA3 & DATA3 \\ \hline DATA3 & DATA3 \\ \hline DATA3 & DATA3 \\ \hline 18 & LVDS_A_CLK & 17 & GND \\ \hline 20 & GND & 19 & LVDS_A_CLH \\ \hline 20 & GND & 21 & LVDS_B \\ \hline DATA0 & 21 & DATA0 \\ \hline DATA0 & 23 & GND \\ \hline 24 & LVDS_B & 23 & GND \\ \hline DATA1 & 25 & DATA1 \\ \hline 26 & GND & 25 & LVDS_B \\ \hline DATA1 & 27 & DATA2 \\ \hline DATA2 & 27 & DATA2 \\ \hline DATA2 & 29 & DPLVDD_EN \\ \hline 30 & LVDS_B & 29 & DPLVDD_EN \\ \hline 34 & LVDS_B CLK & 33 & LVDS_B \\ \hline 34 & LVDS_B CLK & 33 & LVDS_B \\ \hline 36 & CON_LBKLT \\ \hline 38 & LCD_BLT_VCC & 37 & CON_LBKLT \\ \hline CTL & CTL \\ \hline \end{array}$		LVDS_A_		LVDS_A_
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	16	DATA3	15	DATA3#
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	18	LVDS_A_CLK#	17	GND
22 DATA0 21 DATA0# 24 LVDS_B_ DATA1# 23 GND 26 GND 25 LVDS_B_ DATA1 28 LVDS_B_ DATA2 27 DATA2# 30 LVDS_B_ DATA3# 29 DPLVDD_EN DATA3 32 GND 31 LVDS_B_ DATA3 34 LVDS_B_CLK 33 LVDS_B_CLK 36 CON_LBKLT_ EN 35 GND 38 LCD_BLT_VCC 37 CON_LBKLT_ CTL	20	GND	19	LVDS_A_CLK
DATA0DATA0#24IVDS_B_ DATA1#23GND26GND25IVDS_B_ DATA128IVDS_B_ DATA227IVDS_B_ DATA2#30IVDS_B_ DATA3#29DPIVDD_EN32GND31IVDS_B_ DATA334IVDS_B_CLK33IVDS_B_CLK36CON_LBKLT_ EN35GND38ICD_BLT_VCC37CON_LBKLT_ CTL	22	LVDS_B_		LVDS_B_
24 DATA1# 23 GND 26 GND 25 LVDS_B	22	DATA0	21	DATA0#
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		LVDS_B_		CUID
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	24	DATA1#	23	GND
$\begin{array}{c c c c c c c c c c c c c c c c c c c $			25	LVDS_B_
28 DATA2 27 DATA2# 30 LVDS_B_ DATA3# 29 DPLVDD_EN 32 GND 31 LVDS_B_ DATA3 34 LVDS_B_CLK 33 LVDS_B_CLK 36 CON_LBKLT_ EN 35 GND 38 LCD_BLT_VCC 37 CON_LBKLT_ CTL	26			DATA1
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		LVDS_B_		LVDS_B_
30 LVDS_B_ DATA3# 29 DPLVDD_EN 32 GND 31 LVDS_B_ DATA3 34 LVDS_B_CLK 33 LVDS_B_CLK 36 CON_LBKLT_ EN 35 GND 38 LCD_BLT_VCC 37 CON_LBKLT_ CTL	28	DATA2	27	DATA2#
DATA3# Image: Constraint of the state of				
32 GND 31 DATA3 34 LVDS_B_CLK 33 LVDS_B_CLK 36 CON_LBKLT_ EN 35 GND 38 LCD_BLT_VCC 37 CON_LBKLT_ CTL	30	DATA3#	29	DPLVDD_EN
32 GND 31 DATA3 34 LVDS_B_CLK 33 LVDS_B_CLK 36 CON_LBKLT_ EN 35 GND 38 LCD_BLT_VCC 37 CON_LBKLT_ CTL			31	LVDS_B_
34 LVDS_B_CLK 33 LVDS_B_CLK 36 CON_LBKLT_ EN 35 GND 38 LCD_BLT_VCC 37 CON_LBKLT_ CTL	32	GND		
36 CON_LBKLT_ EN 35 GND 38 LCD_BLT_VCC 37 CON_LBKLT_ CTL	34	LVDS_B_CLK	33	LVDS_B_CLK#
EN EN EN 38 LCD_BLT_VCC 37 CON_LBKLT_CTL	21		25	
38 LCD_BLT_VCC 37 CON_LBKLT_CTL	36	EN	35	GND
38 LCD_BLT_VCC 37 CTL			37	CON_LBKLT_
	38	LCD_BLT_VCC		
40 LCD_BLT_VCC 39 LCD_BLT_VC	40	LCD BLT VCC	39	LCD_BLT_VCC

Digital Input /	2 00 0	PIN	Signal Name	PIN	Signal Name
Output Pin Header		10	GND	9	JGPIO_PQR1
(10-pin JGPIO1)(see	ŏŏ]	8	SIO_GP3	7	SIO_GP7
p.13, No. 12)	r <u>□</u> 0	6	SIO_GP2	5	SIO_GP6
		4	SIO_GP1	3	SIO_GP5
		2	SIO_GP0	1	SIO_GP4
UPS Module Power					
Input Connector					
(2-pin DC_UPS1)					
(see p.13, No. 2)					
ATX Power Input/					
Output Connector					
(2-pin INT_DC1)					
(see p.13, No. 1)					
SATA Power					
Output Connector	-				
(SATA_PWR1)					
(see p.13, No. 4)					
RS-232 Port 4 Pin	DDCD#	1			

RS-232 Port 4 Pin Headers (9-pin COM1: see p.13, No. 19) (9-pin COM2: see p.13, No. 20)

CPU Fan Connector (4-pin CPU_FAN1) (see p.13 No. 13)

GN D	
+12V	
CPU_FAN_SPEED	
FAN SPEED CONTRO	

RRXD

TTXD1 GND |

RRTS#1

CCTS#1 | DDSR#1 DDTR# F

NC

Please connect the CPU fan cable to the connector and match the black wire to the ground pin.



Though this motherboard provides 4-Pin CPU fan (Quiet Fan) support, the 3-Pin CPU fan still can work successfully even without the fan speed control function. If you plan to connect the 3-Pin CPU fan to the CPU fan connector on this motherboard, please connect it to Pin 1-3.

Pin 1-3 Connected



3-Pin Fan Installation

Chassis Fan Connector (3-pin CHA_FAN1) (see p.13, No. 28)



GND

SPDIFOUT

FAN_SPEED -

C

+ 12V

GNF

Please connect the fan cable to the fan connector and match the black wire to the ground pin.

SPDIF1

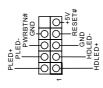
(3-pin SPDIF1: see p.13, No. 25)

VGA2 (10-pin VGA2: see p.13, No. 32)



PIN	Signal Name	PIN	Signal Name
1	RED	2	GND
3	GRN	4	GND
5	BLUE	6	GND
7	HSYNC	8	VSYNC
9	DDC_CLK	10	DDC_DATA

System Panel Header (9-pin PANEL1) (see p.13, No. 15)



This header accommodates several system front panel functions.



PWRBTN (Power Switch):

Connect to the power switch on the chassis front panel. You may configure the way to turn off your system using the power switch.

RESET (Reset Switch):

Connect to the reset switch on the chassis front panel. Press the reset switch to restart the computer if the computer freezes and fails to perform a normal restart.

PLED (System Power LED):

Connect to the power status indicator on the chassis front panel. The LED is on when the system is operating. The LED keeps blinking when the system is in S3 sleep state. The LED is off when the system is in S4 sleep state or powered off (S5).

HDLED (Hard Drive Activity LED):

Connect to the hard drive activity LED on the chassis front panel. The LED is on when the hard drive is reading or writing data.

The front panel design may differ by chassis. A front panel module mainly consists of power switch, reset switch, power LED, hard drive activity LED, speaker and etc. When connecting your chassis front panel module to this header, make sure the wire assignments and the pin assignments are matched correctly.

SATA2 Connectors (SATAII_1/SATAII_2: see p.13, No. 33)



These two Serial ATA2 (SATA2) connectors support SATA data cables for internal storage devices. The current SATA2 interface allows up to 3.0 Gb/s data transfer rate.

3W Audio Amp Output Wafer (4-pin SPEAKER1) (see p.13, No. 27)



PIN	Signal Name
1	SPK L-
2	SPK L+
3	SPK R+
4	SPK R-

USB 2.0 Headers (9-pin USB4_5: see p.13, No. 16) (9-pin USB6_7: see p.13, No. 17)

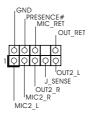


Besides four default USB 2.0 ports on the I/O panel, there are two USB 2.0 headers on this motherboard. Each USB 2.0 header can support two USB 2.0 ports. Chassis Intrusion Headers (2-pin CI1/CI2: see p.13, No. 29)



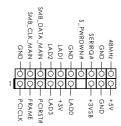
This motherboard supports CASE OPEN detection feature that detects if the chassis cover has been removed. This feature requires a chassis with chassis intrusion detection design.

Front Panel Audio Header (9-pin HD_AUDIO1) (see p.13 No. 26)



This is an interface for front panel audio cable that allows convenient connection and control of audio devices.

TPM Header (17-pin TPM1) (see p.13, No. 23)



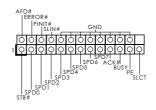
This connector supports a Trusted Platform Module (TPM) system, which can securely store keys, digital certificates, passwords, and data. A TPM system also helps enhance network security, protects digital identities, and ensures platform integrity.

PS2_KB_MS1 (8-pin PS2_KB_MS1) (see p.13, No. 21)



PIN	Signal Name
1	KBCLK
2	+5V
3	KBDATA
4	+5V
5	MSDATA
6	GND
7	MSCLK
8	GND

Print Port Header (25-pin LPT1) (see p.13, No. 22)



This is an interface for print port cable that allows convenient connection of printer devices.

DMIC1 (4-pin DMIC1) (see p.13, No. 18)

1	0	0	Ο	Ο	
					_

PIN	Signal Name
1	+3V
2	DMIC_DATA
3	GND
4	DMIC_CLK
5	NC

CS1 (9-pin CS1) (see p.13, No. 24)

000 **D** 00000

PIN	Signal Name
1	Watch Dog Timer
2	Ground
3	NC
4	SMB_CLK_
4	RESUME
5	+3.3V standby
6	SMB_DATA_
0	RESUME
7	PWRBT#
8	CIRRX
9	+5.0V standby
10	Ground

4.5 Expansion Slots (PCI Express, mini-PCIe and mini-PCIe/

mini-SATA Slots)

There is 1 PCI Express slot, 1 mini-PCIe slot and 1 mini-PCIe/mini-SATA slot on this motherboard.



Before installing an expansion card, please make sure that the power supply is switched off or the power cord is unplugged. Please read the documentation of the expansion card and make necessary hardware settings for the card before you start the installation.

PCIe slot:

PCIE1 (PCIE x1 slot) is used for PCI Express x1 lane width graphics cards.

mini-PCIe slot:

MINI_PCIE2 (mini-PCIe slot; half size) is used for PCI Express mini cards

mini-PCIe/mini-SATA slot:

MINI_PCIE1 (mini-PCIe/mini-SATA slot; full size) is used for PCI Express mini cards or mSATA cards.